CLAIMS:

What is claimed is:

1. A partly reprogrammable Finite State Machine including a state register holding the current state and two functions *(of* and *nf*) comprising combinational logic to calculate the outputs and the next state, respectively, said combinational functions being representable in a "sum of product terms form", said Finite State Machine comprising:

a) a circuit disabling a predetermined number of product terms associated with said "sum of product terms form", each product term corresponding to a given state and a given input vector setting,

b) a circuit enabling a new product term for a predetermined respective number of new product terms generating for each, a correct output signal corresponding to a given error state and a given error input bit vector, and

c) said disabling and /or enabling circuits being provided in a form which allows activation thereof in case a product term was tested to include a bug.

2. The state machine according to claim 1, in which the circuit disabling a predetermined number of product terms comprises a control latch, the output of which connects to a logical AND gate, the input signals of which further comprise signal lines associated with the error state and the respective input vector.

3. The state machine according to claim 1, in which the circuit disabling a predetermined number of product terms comprises a respective number of disable registers, each associated with a respective decoder.

4. The state machine according to claim 1, in which the circuit enabling a new product term comprises:

a) an input mask register,

b) an input compare register,

c) a state compare register, and

d) an output register, which holds the corrected output signals.

5. The state machine according to claim 4 which further comprises a next state register, which holds the output signals for the next state.

6. The state machine according to claim 1, further comprising:

a) circuit disabling an error-comprising otherwise logic, and

b) circuit enabling a new corrected otherwise logic, which comprises logic reflecting enabled new product terms.

7. The state machine according to claim 1 in which,

the circuit disabling a predetermined number of product terms, the circuit enabling a predetermined respective number of new product terms and a corrected output signal vector are programmed in a content addressable memory, and

whereby the error state and the error input vector is used as a search argument into said content addressable memory.

8. The state machine according to claim 1 in which the circuit enabling a new product term comprises a Random Access Memory (RAM) including logic creating a corrected output vector, and a RAM address generation logic is provided for selectively accessing respective RAM entries, and a state machine select logic is provided for selecting between activation of either the regular state machine or the RAM for generating a desired output vector.

9. The state machine according to claim 8 in which the RAM comprises a plurality of compartments, each of them comprising input mask logic, input compare logic, next state logic and correct product term output signal logic, respectively.